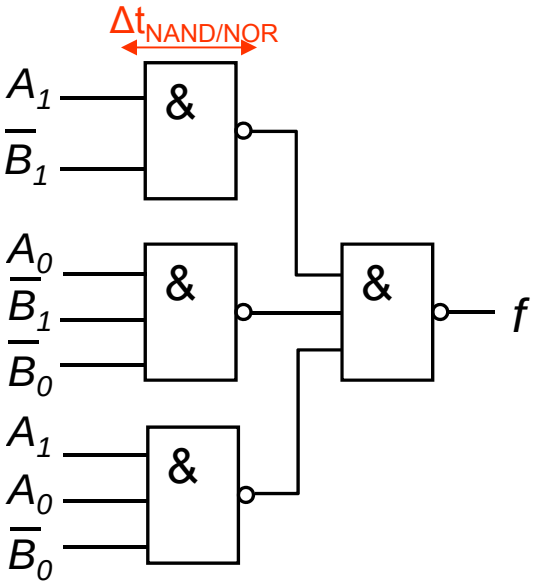
Digitalne strukture
3. Vaja

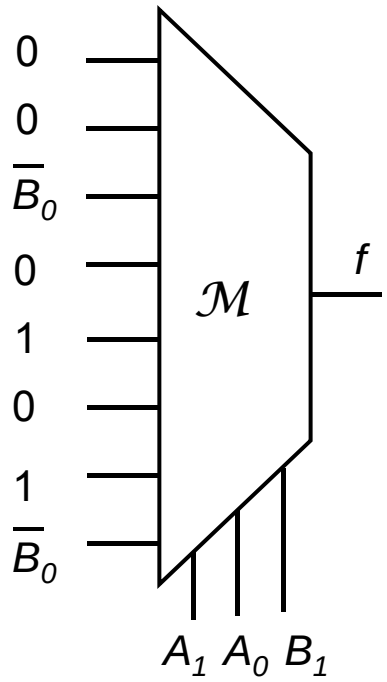
Simulacija delovanja kombinacijskih vezij (P-SPICE)

Naloga 3a: Simulacija dvobitnega primerjalnika z NAND/NOR:



Naloga 3b: Zakasnitev (“propagation delay”) vrat NAND/NOR - $\Delta t_{NAND/NOR}$

Naloga 3c: Simulacija dvobitnega primerjalnika z multipleksorjem 74HC151:



Naloga 3d: Statični hazard v vezjih AND-OR oz. OR-AND:

$$f(x_1, x_2, x_3) = \sum 0, 2, 3, 7$$

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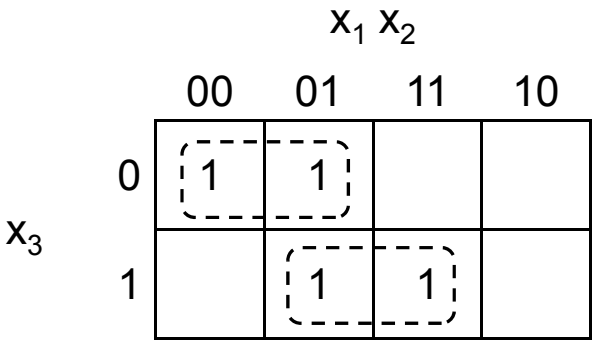

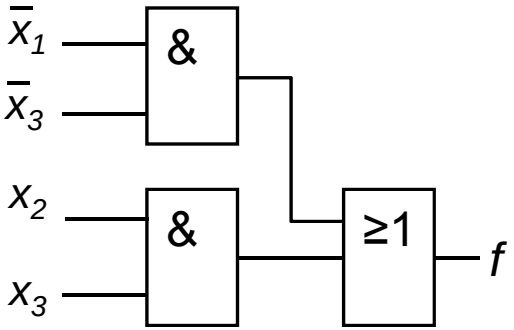

Časovni diagram: pri kateri spremembi vhodov se pojavi hazard?

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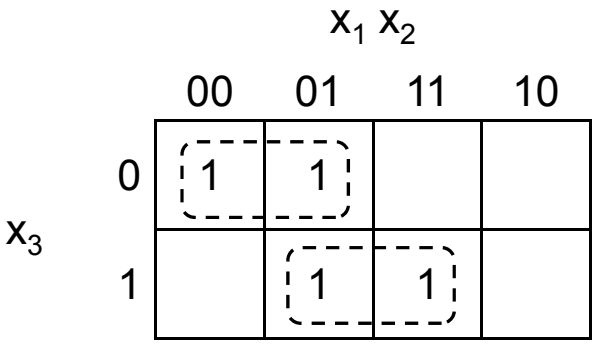
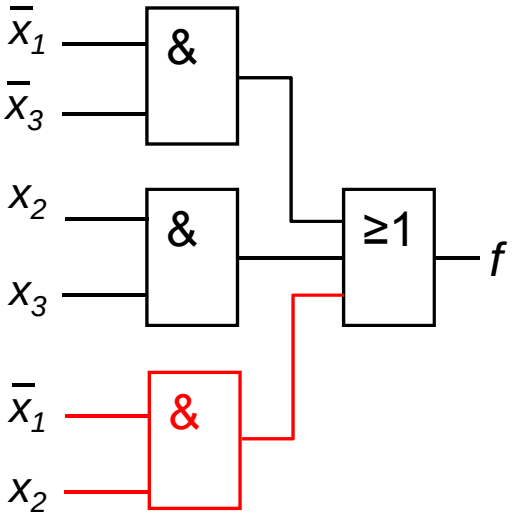
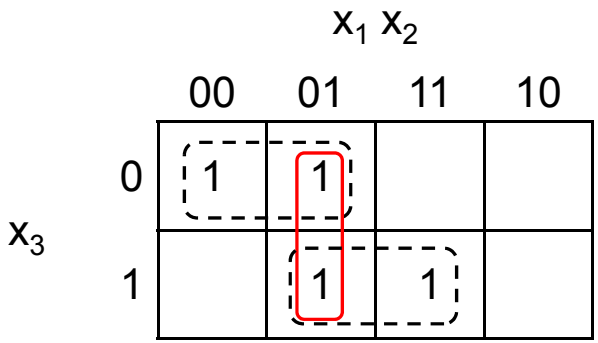
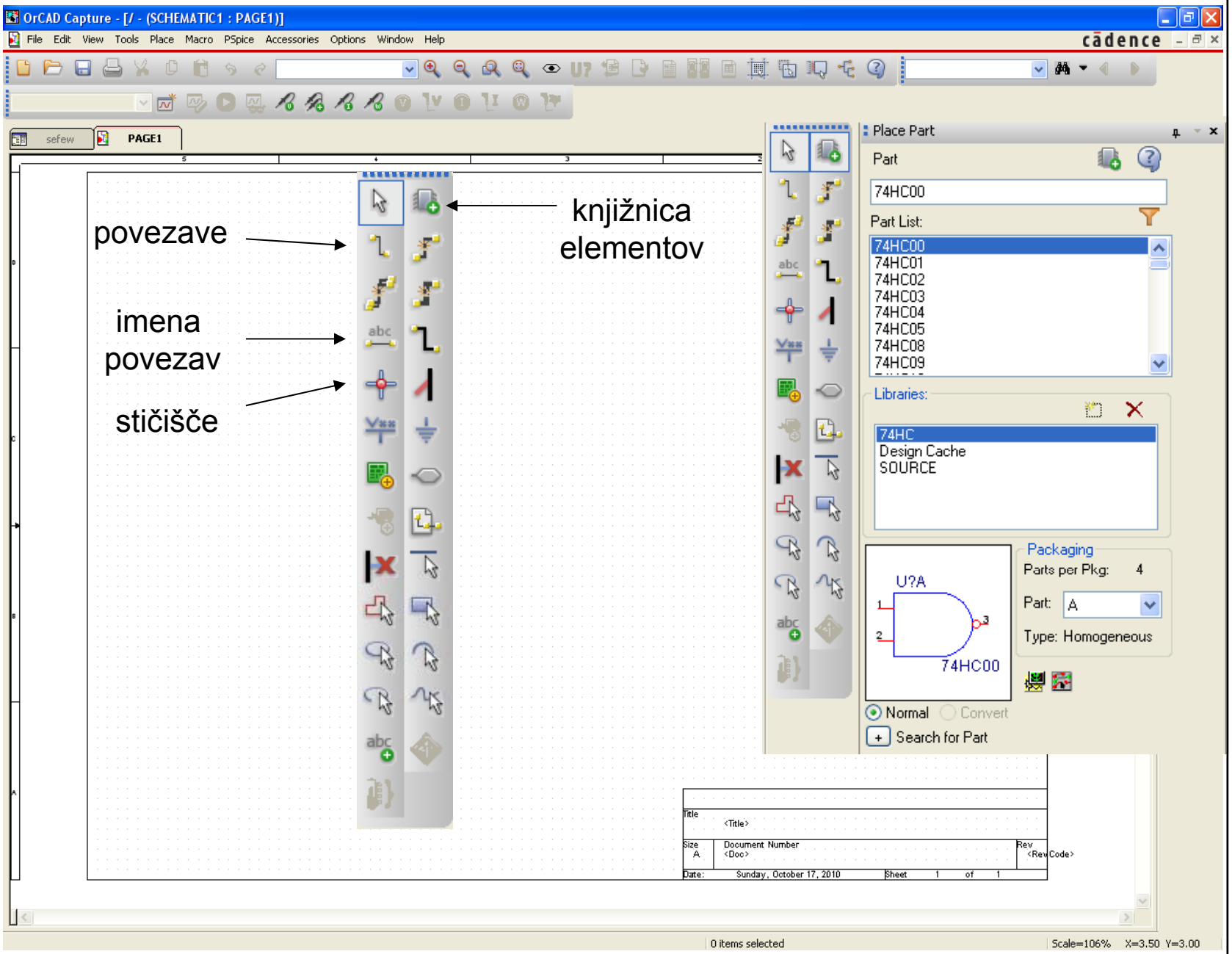




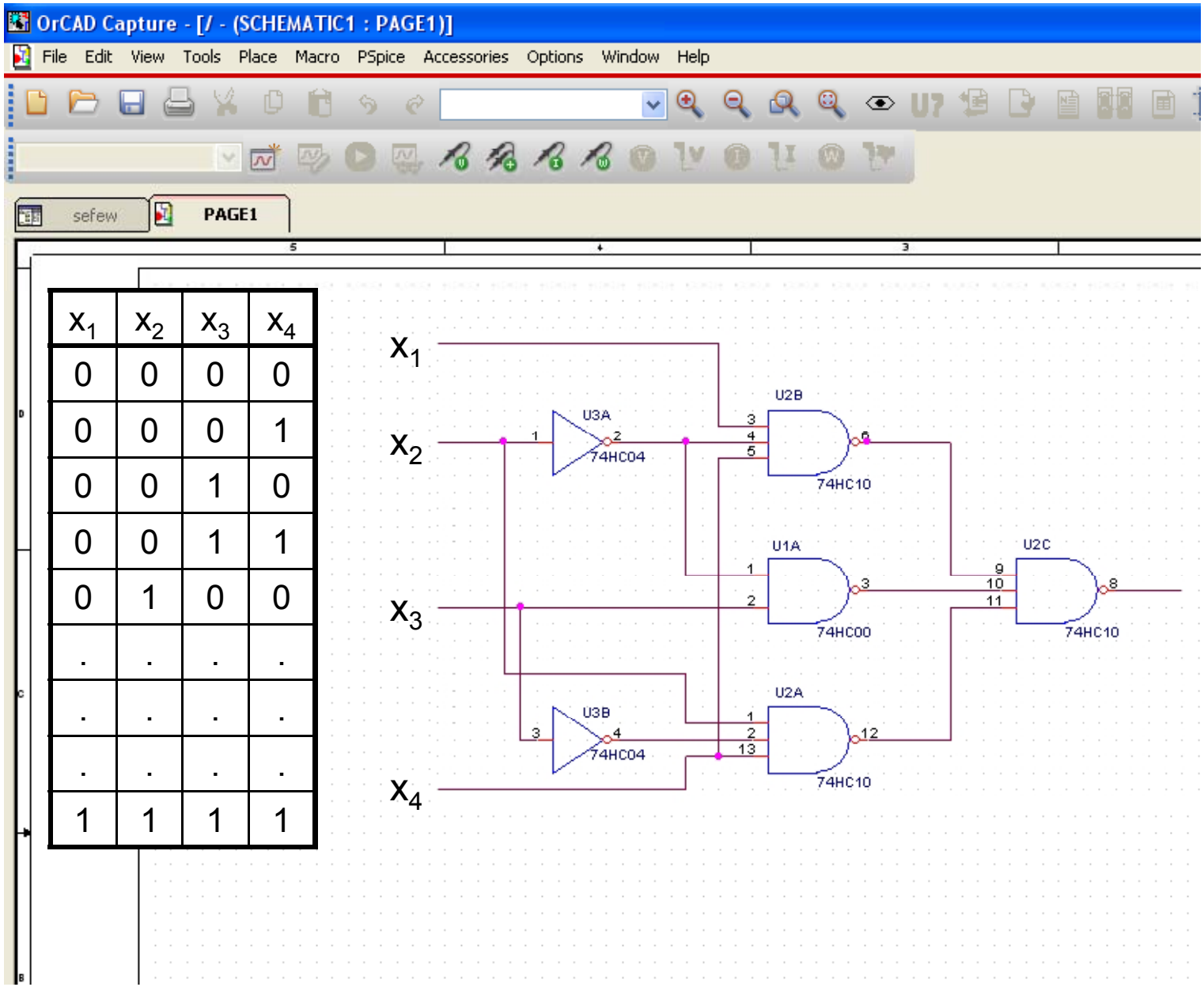
Naloga 3e: Odprava hazarda:



OrCAD (PSpice)

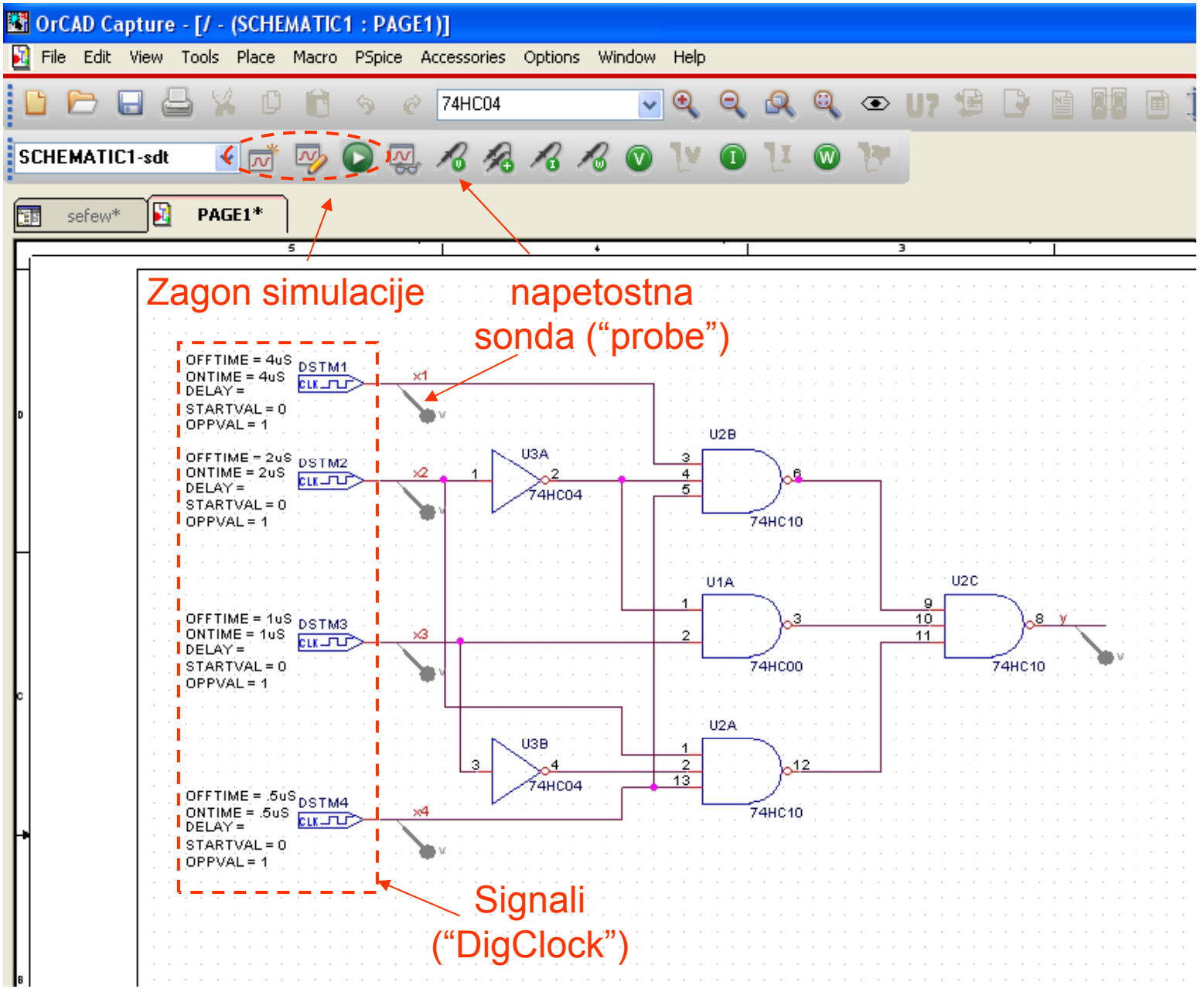


Vezje

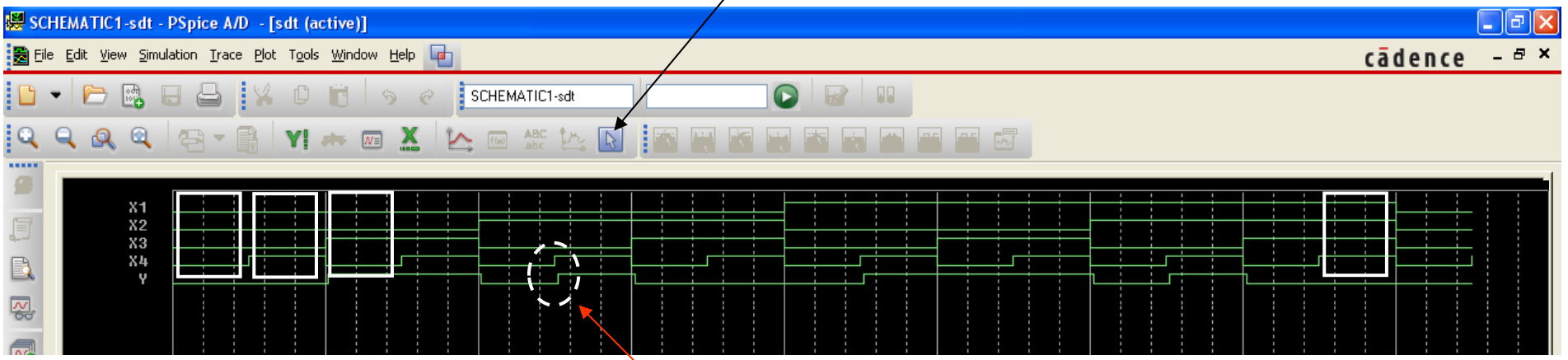


x_1	x_2	x_3	x_4
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
.	.	.	.
.	.	.	.
.	.	.	.
1	1	1	1

Vhodni signali in sonde



Rezultati simulacije (časovni diagram)



x_1	x_2	x_3	x_4	y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
.	.	.	.	
.	.	.	.	
.	.	.	.	
1	1	1	1	0

Poročilo

- Besedilo vaje
- Časovni diagram vhodnih in izhodne spremenljivke (*primerjalnik*)
- Zakasnitev na vratih NAND/NOR
- Časovni diagram izhodne funkcije vezja s hazardom