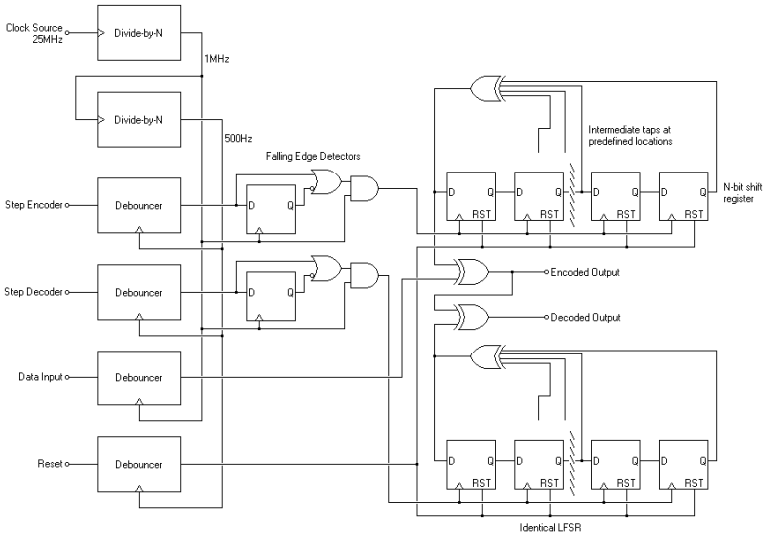
Digitalna tehnika
4. Vaja

Opis vezij z VHDL

Načrtovanje digitalnih vezij:

- ponavadi shematsko (nivo logičnih vrat, tranzistorjev, registrov)
- pri kompleksnih vezjih zaradi večje preglednosti uporabimo strojno opisne jezike



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```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity prim is
   Port ( A : in  STD_LOGIC_VECTOR (1 downto 0);
          B : in  STD_LOGIC_VECTOR (1 downto 0);
           f : out  STD_LOGIC);
end prim;

architecture Behavioral of prim is
signal f1, f2, f3: std_logic;
begin
  f1<= A(1) or (not B(1));
  f2<= A(1) or A(0) or (notB(0));
  f3<= A(0) or (not B(1)) or (not B(0));
    f<= f1 and f2 and f3;
end Behavioral;
```

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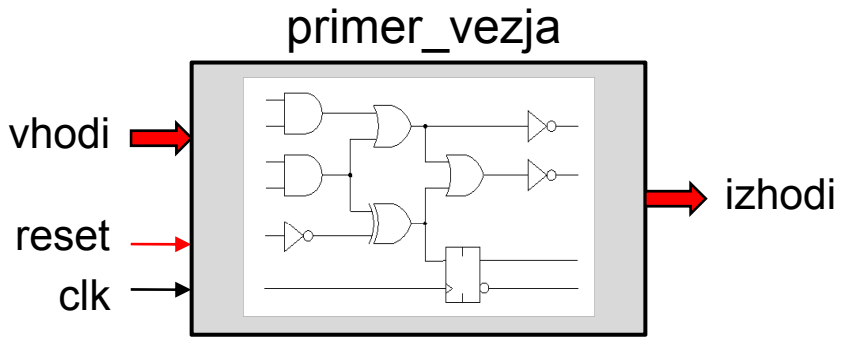
- ponavadi shematsko (nivo logičnih vrat, tranzistorjev, registrov)
- pri kompleksnih vezjih zaradi večje preglednosti uporabimo strojno opisne jezike

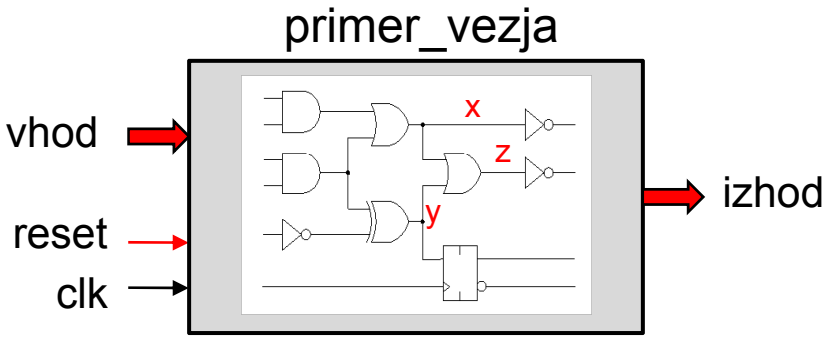
Strojno opisni jeziki: jeziki za simulacijo in opis digitalnih vezij (VHDL, Verilog, Abel,…)

VHDL: Very High Speed Integrated Circuit Hardware Description Language
(jezik za opis zelo hitrih digitalnih vezij)

Model vezja v VHDL:



Model vezja v VHDL:



➢ vmesnik (*entity*)

```
entity primer_vezja is
port (vhod: in std_logic_vector (3 downto 0);
  reset, clk: in std_logic;
        izhod: out std_logic_vector (3 downto 0));
end primer_vezja;
```

➢ zgradba (*architecture*)

```
architecture opis of primer_vezja is
signal x, y, z: std_logic;
begin
x<= (vhod(0) and vhod(1)) or (vhod(2) and vhod(3));
izhod (0)<= not(x);
:
end opis;
```

4a) Enobitni primerjalnik

VHDL:
f<= x_1 and not (x_2);

4b) Dvobitni primerjalnik

Izhajajte iz oblike MDNO, vpeljite nove spremenljivke:

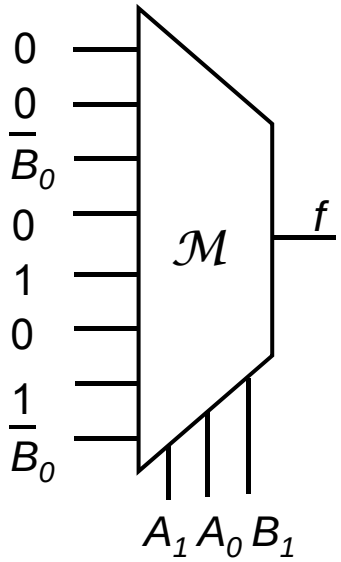
npr: $f(x_1,x_2,x_3) = x_1x_2 + x_2\overline{x}_3 = w+y$

VHDL:
signal w, y: std_logic;
f<= w or y;
w<= x_1 and x_2 ;
y<= x_2 and not (x_3);

4c) Primerjalnik z multipleksorjem

Uporabite stavek *when…else*

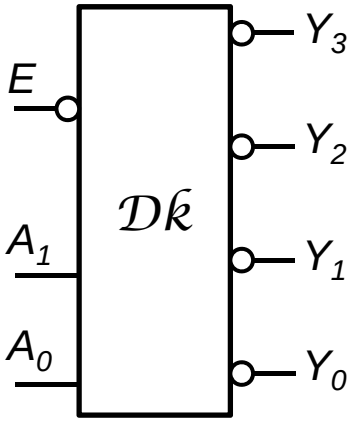
```
ime_spremenljivke<= vrednost1 when izraz1 else
                    vrednost2 when izraz2 else
                       …
                    vrednost n;
```



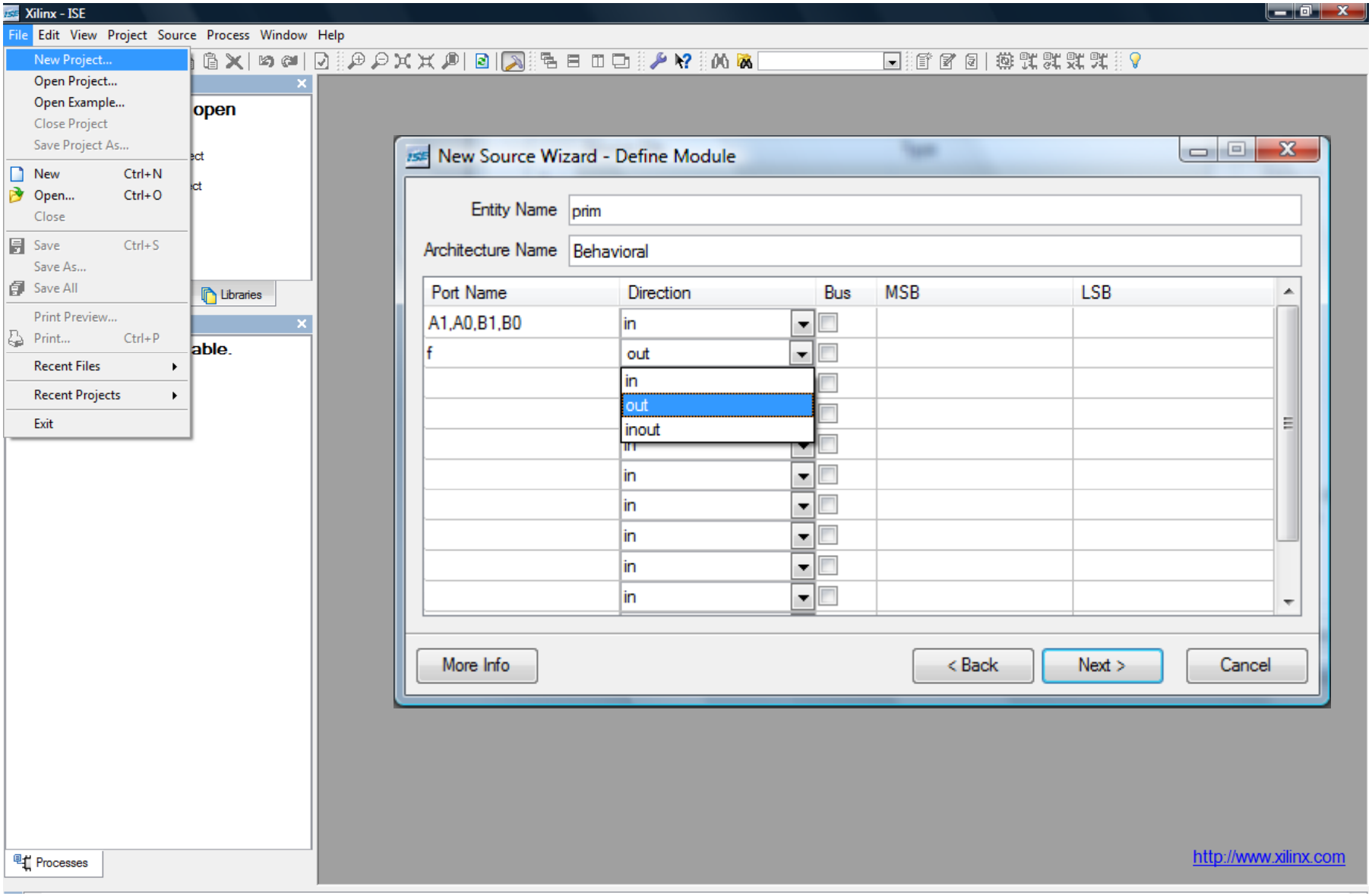
4d) Dekodirnik 2-4

Uporabite stavek *with…select…when*

```
with ime_izbirnega_signala select
     ime_spremenljivke <= vrednost 1 when izbor 1,
                          vrednost 2 when izbor 2,
                             …
                          vrednost n when others;
```



Xilinx ISE – Programiranje FPGA



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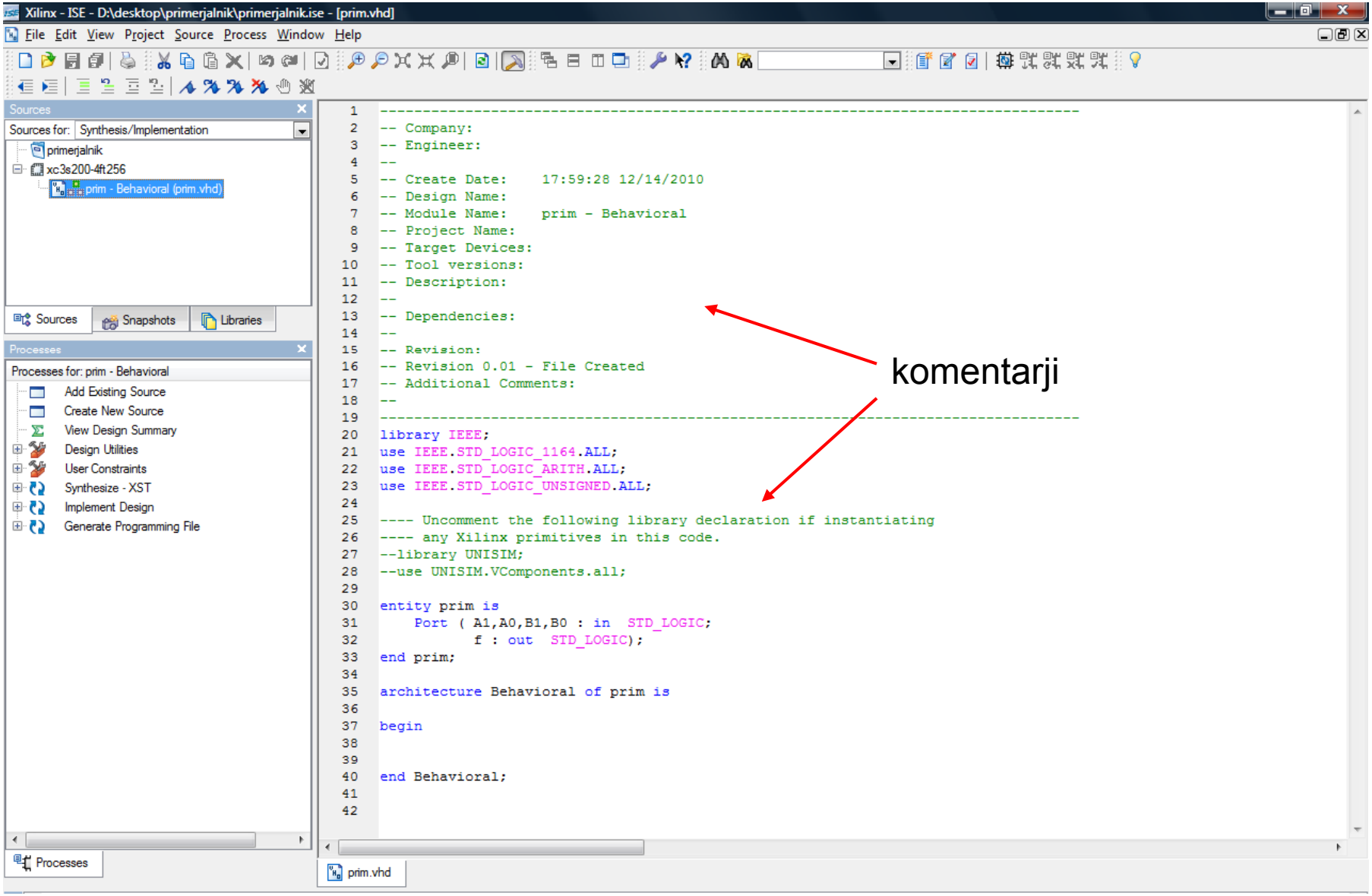
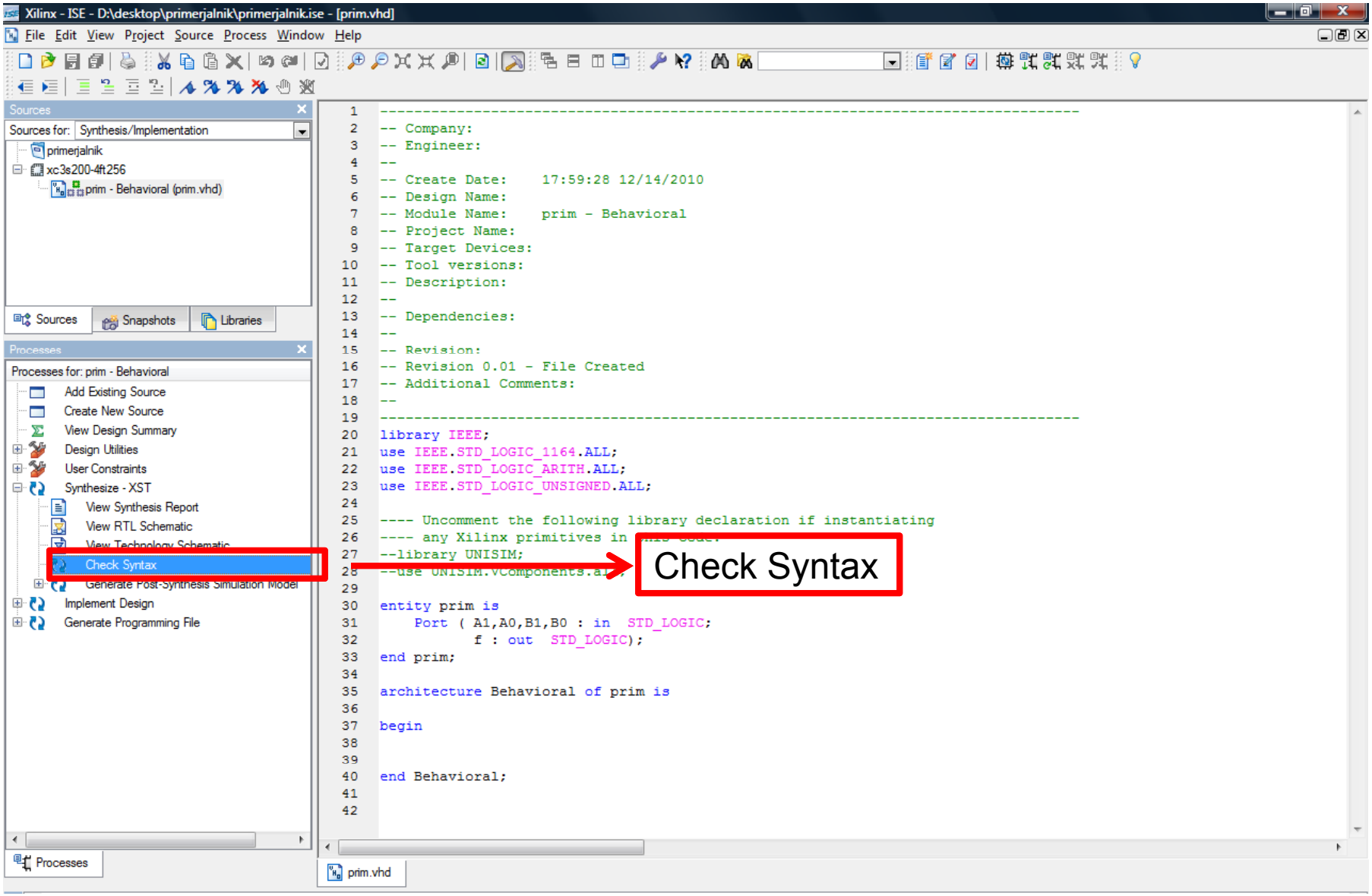



```
1  ----------------------------------------------------------------------------------
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    17:59:28 12/14/2010
6  -- Design Name:
7  -- Module Name:    prim - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------------------------------------------------------------------------------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.STD_LOGIC_ARITH.ALL;
23 use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25 ---- Uncomment the following library declaration if instantiating
26 ---- any Xilinx primitives in this code.
27 --library UNISIM;
28 --use UNISIM.VComponents.all;
29
30 entity prim is
31     Port ( A1,A0,B1,B0 : in  STD_LOGIC;
32            f : out  STD_LOGIC);
33 end prim;
34
35 architecture Behavioral of prim is
36
37 begin
38
39
40 end Behavioral;
41
42
```

Xilinx ISE – Programiranje FPGA



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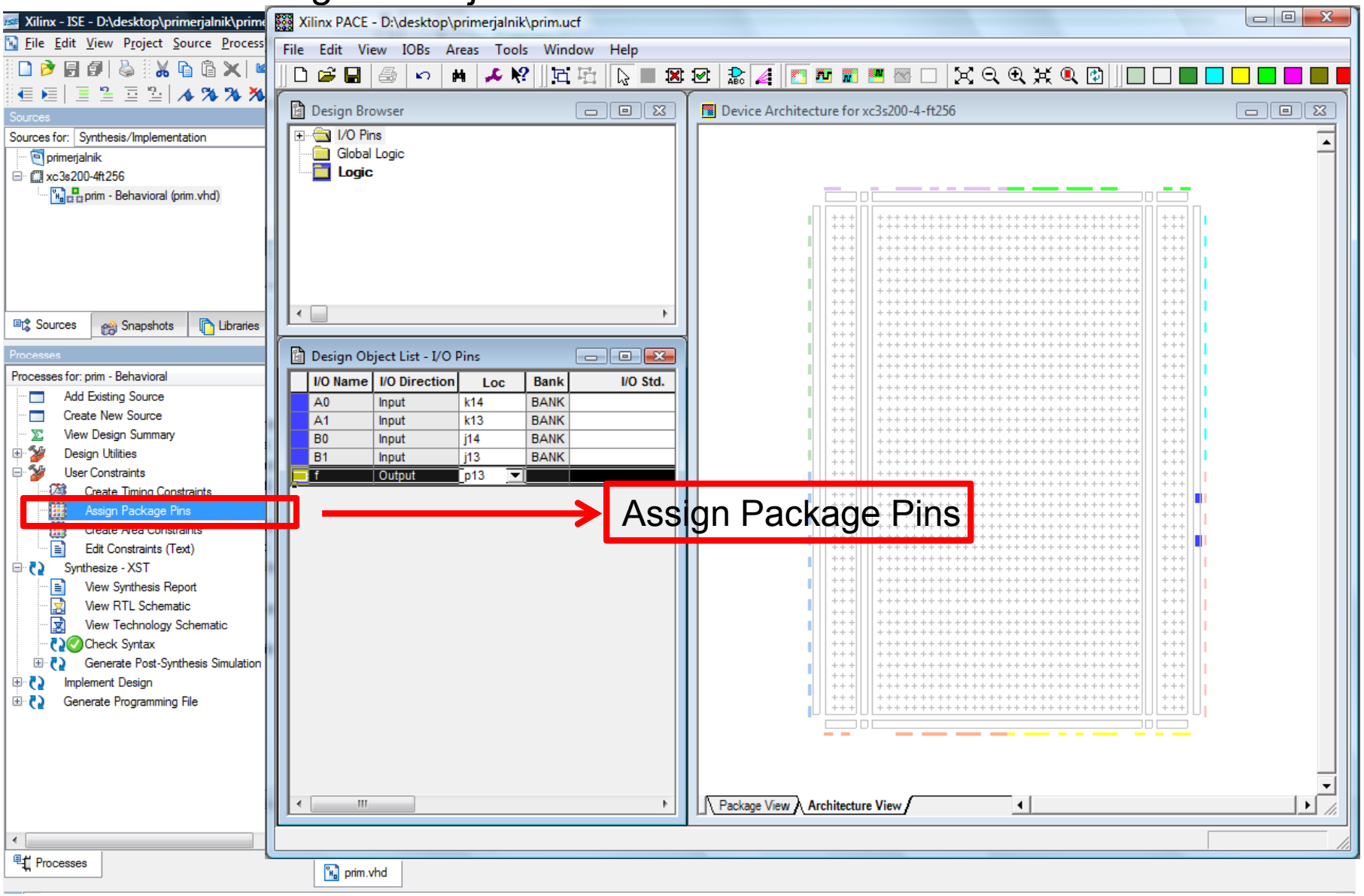

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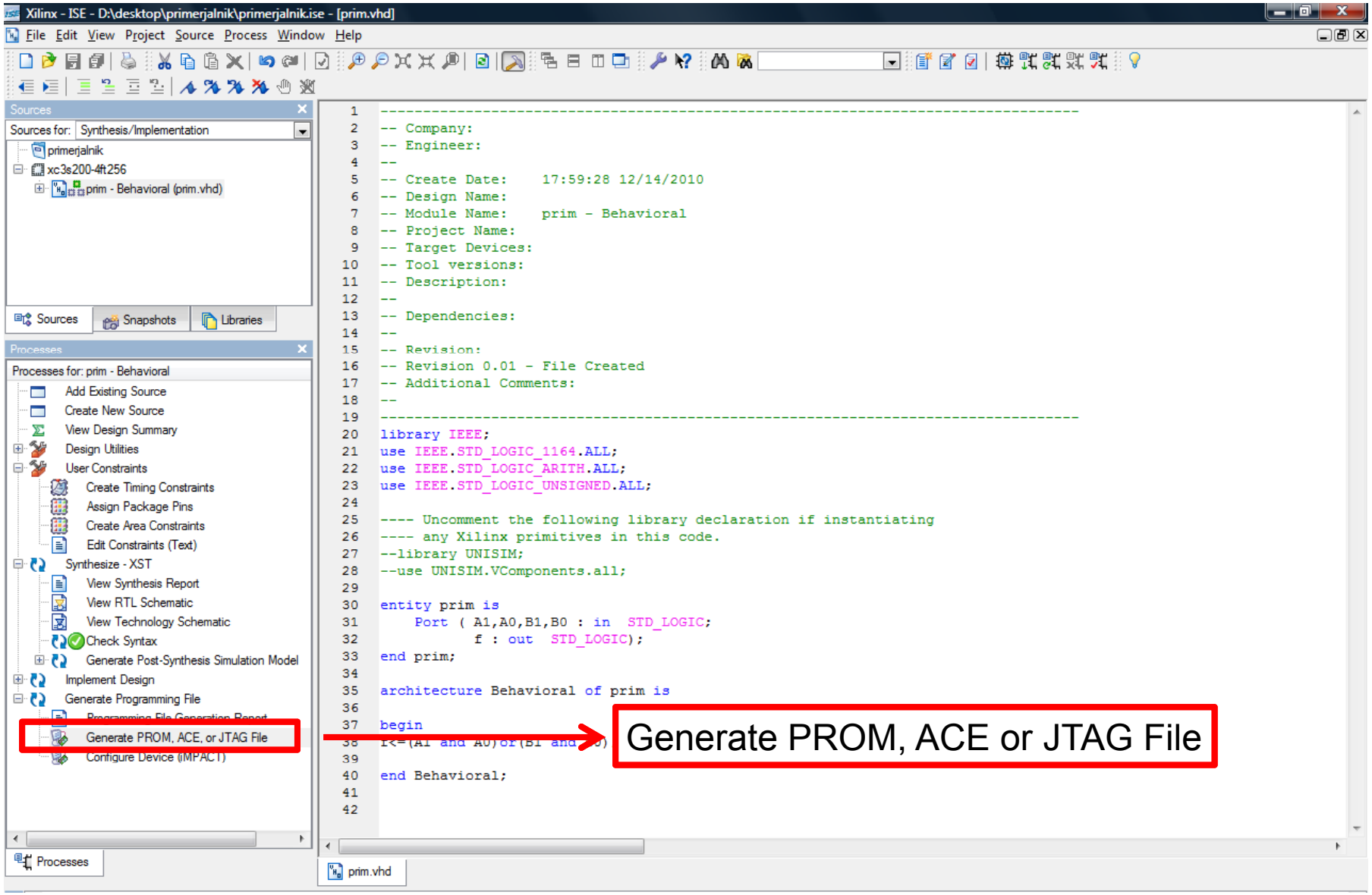

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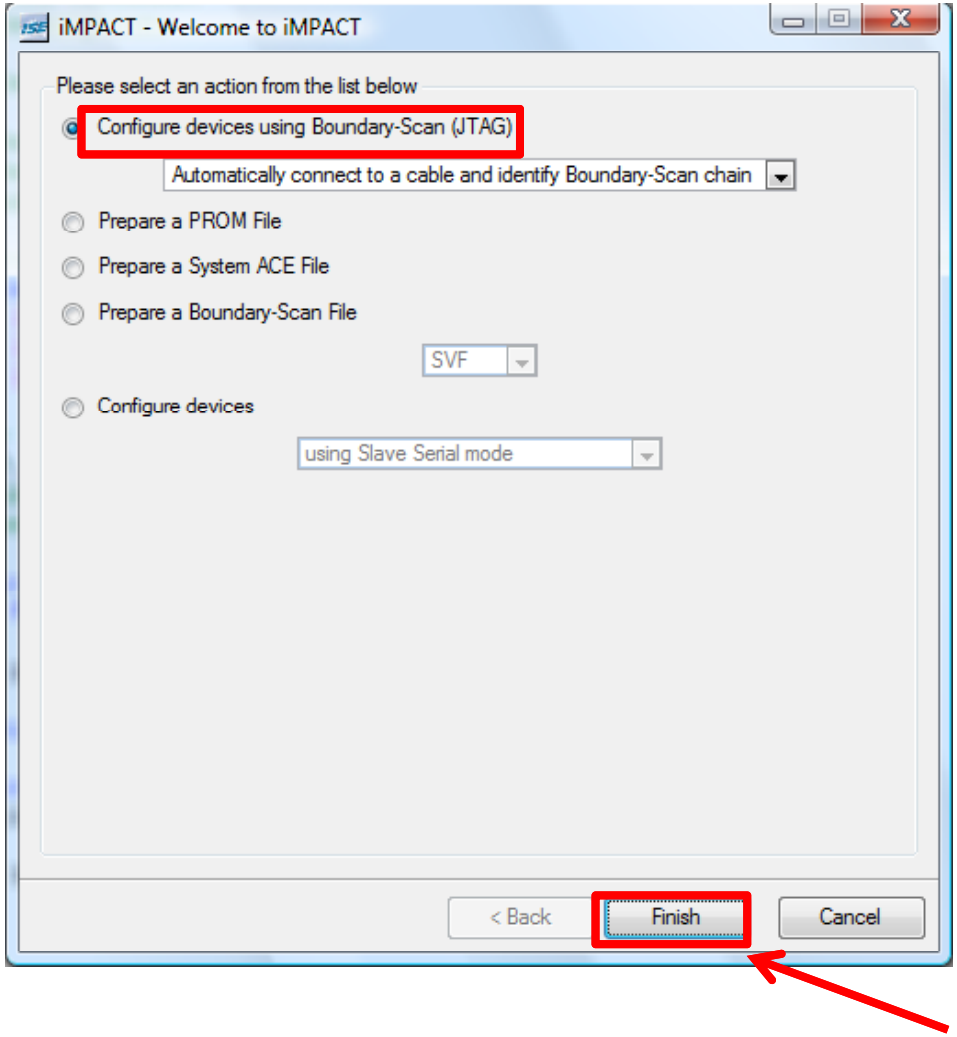

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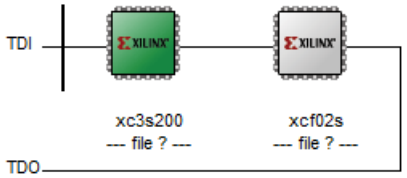

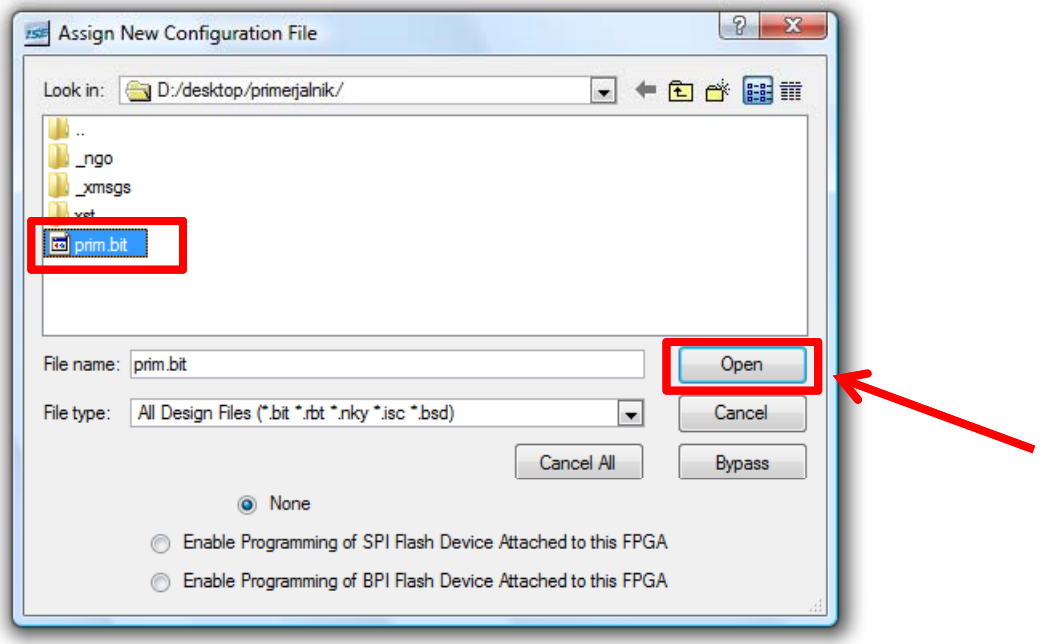

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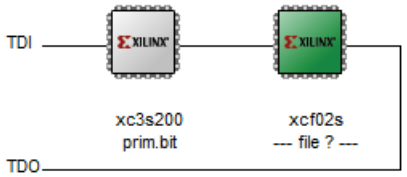
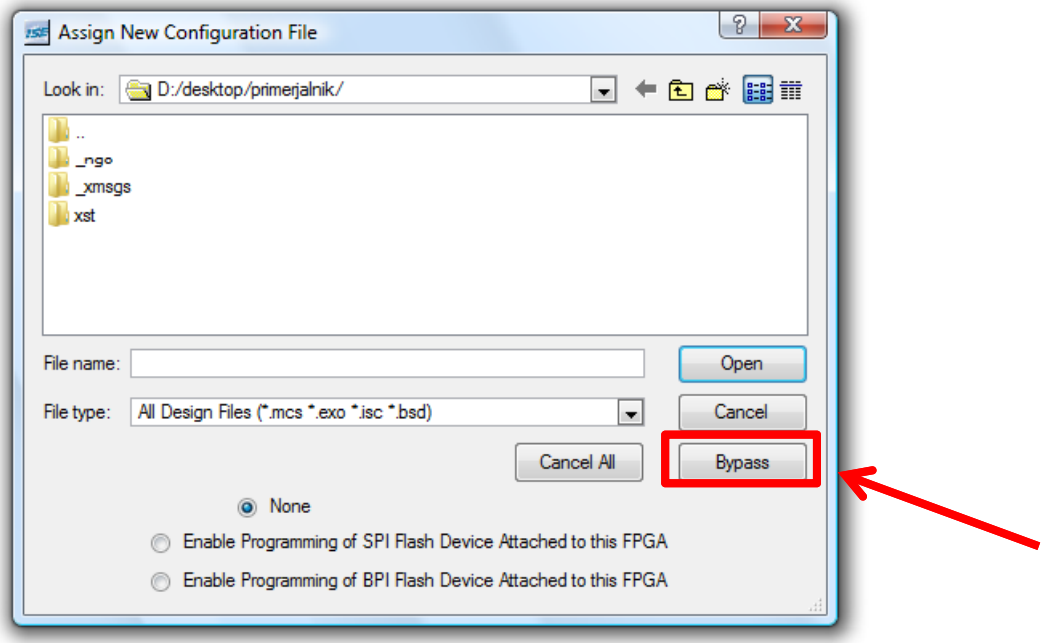
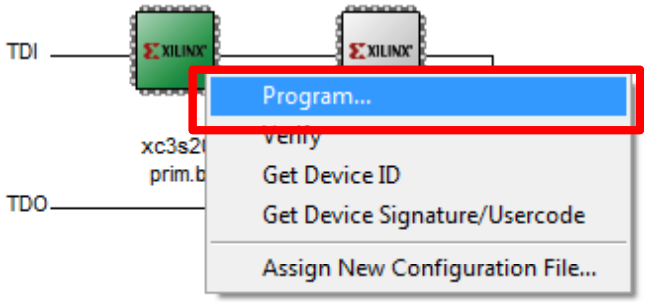




Xilinx ISE – Programiranje FPGA

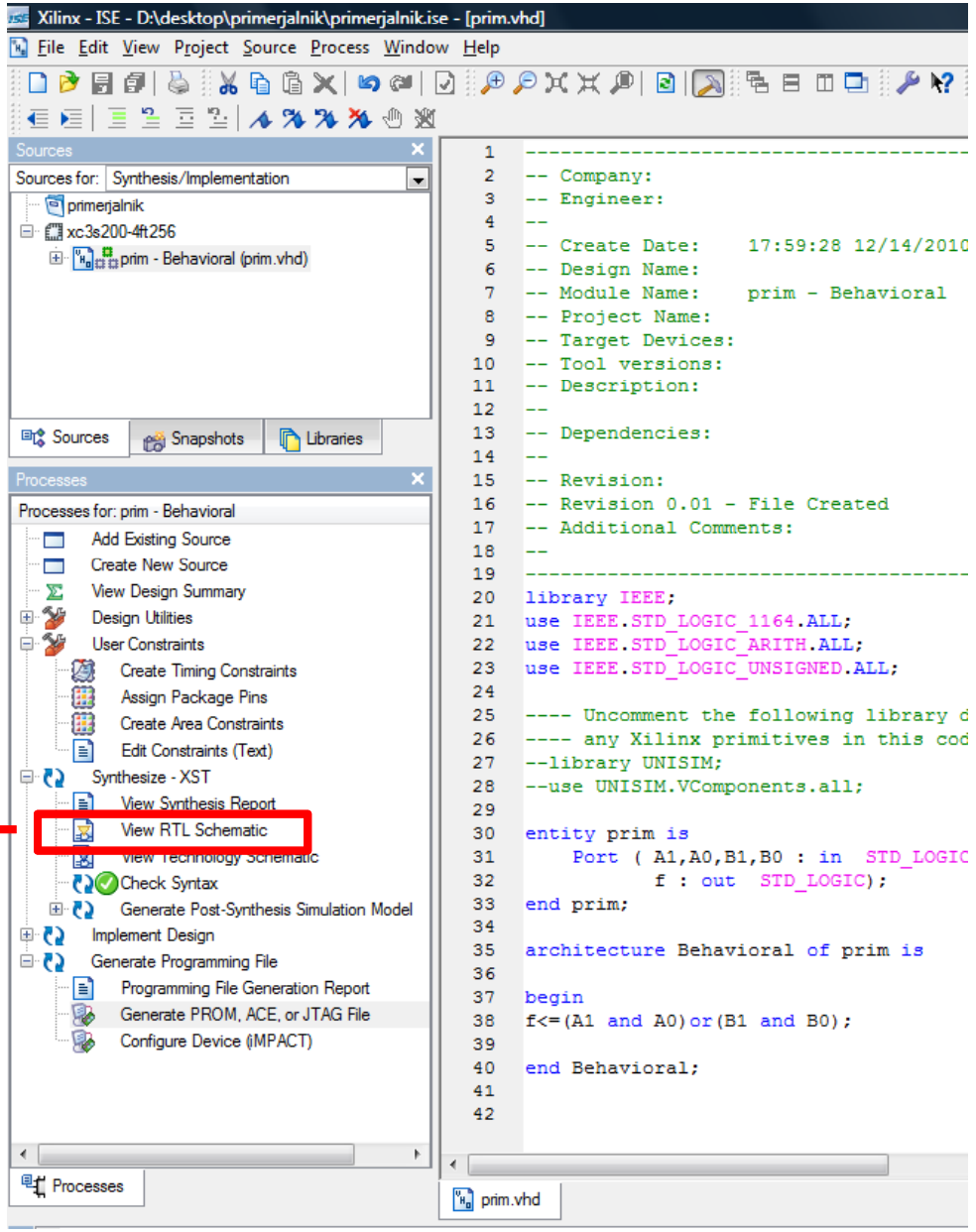
Desni klik na vezje xc3s200



Poročilo

- Besedilo vaje
- VHDL koda za vsako nalogo
- RTL shematika

View RTL Schematic



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